

CLAIMS

What is claimed is:

1           1.     An optical transfer system for converting an externally-applied video  
2     signal into an optical signal and for restoring the optical signal to the original video  
3     signal, the system comprising:

4                 a video controller for separating color signals and a horizontal/vertical  
5     synchronous signal from an original video signal, and for transmitting the color signals  
6     and the horizontal/vertical synchronous signal in response to externally-applied  
7     predetermined data enable signal and clock signal;

8                 a transmitter for skew-compensating and compressing signals received from the  
9     video controller and for converting the compressed signals to a driving current;

10                a transmission photo diode for converting the driving current to an optical signal  
11     and for outputting the optical signal;

12                an optical transmission line comprised of a predetermined number of channels,  
13     for transmitting the optical signal;

14                a reception photo diode for converting the optical signal received from the  
15     optical transmission line into a current signal and for outputting the current signal; and

16                a receiver for converting the current signal into a voltage signal, for  
17     decompressing the voltage signal, for compensating for the skew of the voltage signal,  
18     and for restoring the original signal.

1           2.     The optical transfer system of claim 1, wherein the transmitter comprises:  
2                 a phase locked loop for generating a clock signal synchronized with an  
3     externally-generated clock signal, and for outputting the synchronized clock signal to  
4     serve as a clock signal for data transmission;  
5                 a skew compensator for receiving data, each data having a predetermined  
6     number of bits, from the video controller, in response to the synchronized clock signal,

7 via different channels, and compensating for a skew which is generated between the  
8 channel data in response to the synchronized clock signal;

9 a scrambler for counting the number of high levels and the number of low levels  
10 of each of the skew-compensated channel data, and adding the counted information to  
11 each of the channel data to serve as direct current balance information, and  
12 transmitting the resultant data;

13 a data serialization unit for compressing the scrambled channel data in response  
14 to the synchronized clock signal to obtain 1-bit channel data; and

15 an optical driver for receiving the compressed channel data and the clock signal  
16 as different channel data and converting the received data into current signals, in order  
17 to drive the transmission photo diode.

18 3. The optical transfer system of claim 2, wherein the optical driver  
19 comprises:

20 a bias and modulation resistance variation unit including a bias resistor and a  
21 modulation resistor, the resistance value of each of which is variable, for varying a  
22 current amount, which is output due to variations in the resistance values of the bias  
23 resistor and the modulation resistor;

24 a bandgap circuit for determining a bandgap reference voltage, which is  
25 maintained to a constant value independently of external changes, and for varying a  
26 bias current or a modulation current according to the determined reference voltage and  
27 current variations due to variations in the resistance of the bias resistor and the  
28 modulation resistor; and

29 a laser driver for converting received channel data into current signals and for  
30 adding the modulation current and bias current of the current signals to obtain a driving  
31 current for driving external optical devices.

1           4.     The optical transfer system of claim 3, wherein the bandgap circuit  
2 comprises:

3           a bandgap reference voltage generator for compensating according to a  
4 variation in the voltage of a first node, which is a basis for voltage determination, so  
5 that the voltage of the first node maintained at a constant value, and for operationally  
6 amplifying the bandgap reference voltage and a voltage at the modulation resistor  
7 while operationally amplifying the bandgap reference voltage and a voltage at the bias  
8 resistor, thereby to obtain first and second output voltages, respectively;

9           a bias and modulation current generator for constantly maintaining the first and  
10 second output voltages and the voltages at the modulation resistor and the bias  
11 resistor by feeding the first and second output voltages back to the bandgap reference  
12 voltage generator, and for varying the modulation or bias current in response to the  
13 voltages at the modulation resistor or the bias resistor; and

14           a power save controller having at least one switch, which is switched in  
15 response to an externally-input power save control signal, for converting the modes of  
16 the bandgap reference voltage generator and the bias and modulation current  
17 generator into sleep modes in response to the switching of the switches.

1           5.     The optical transfer system of claim 3, wherein the laser driver comprises:  
2           a data separation unit for splitting the channel data into a non-inverted signal  
3 and an inverted signal to obtain a non-inverted output signal and an inverted output  
4 signal; and

5           a voltage-to-current conversion and current driving unit for calculating the  
6 voltage difference between the non-inverted output signal and the inverted output  
7 signal to obtain a current corresponding to the voltage difference, and for adding the  
8 current to the bias current and the modulation current to obtain the driving current.

1           6.     The optical transfer system of claim 1, wherein the receiver comprises:

2 an optical receiver for converting current signals received from the reception  
3 photo diode into voltage signals, and for duty-compensating and level-converting the  
4 voltage signals to obtain digitalized signals which are different channel data; and  
5 a phase locked loop for generating a clock signal which synchronizes with a  
6 clock signal included in the channel data, and for outputting the synchronized clock  
7 signal to serve as an actual clock signal for data reception;

8 a data restoration and skew compensation unit for receiving channel data that  
9 has been compressed by the transmitter, for decompressing the compressed data in  
10 response to the synchronized clock signal, and for skew-compensating the  
11 decompressed data to obtain different channel data each having a predetermined  
12 number of bits; and

13 a descrambler for descrambling in response to the direct current balance  
information in each of the channel data, so that the low level and high level of the  
channel data balance with each other.

7. The optical transfer system of claim 6, wherein the optical receiver  
comprises:

a bias circuit for receiving a predetermined amount of current from a power  
supply voltage and generating first and second bias currents;

a current-to-voltage converter for sourcing a current in response to the first bias  
current and converting a current signal received from the reception photo diode into a  
differential voltage signal;

an amplifier for sourcing a current in response to the first bias current and  
amplifying the differential voltage signal to obtain first and second differential output  
signals;

a duty compensator realized with different comparators having a current  
summing structure in which output currents are summed, the duty compensator for  
sourcing a current in response to the first bias current and comparing the first

14 differential output signal with a first reference voltage and the second differential output  
15 signal with a second reference voltage to obtain first and second output signals which  
16 correspond to the compared results;

17 a level converter for sourcing a current in response to the second bias current  
18 and digitalizing the first and second output signals by converting the voltage levels of  
19 the first and second output signals; and

20 a buffer unit for buffing and amplifying signals received from the level converter  
21 to obtain the digital channel data.

1 8. The optical transfer system of claim 6, wherein the optical receiver further  
2 comprises a power down controller for powering down the bias circuit so that it does not  
3 operate, in response to an externally-applied power down control signal.

4 9. The optical transfer system of claim 6, wherein the data restoration and  
5 skew compensation unit comprises:

6 a first latch unit for latching data received in series from the optical receiver, in  
7 units of  $n+N-1$  (where  $N$  is a positive integer greater than or equal to 3) bits in parallel  
8 in response to first through  $n$ -th non-overlapped clock signals, and outputting  $N$   $n$ -bit  
9 latched state data having the time difference of a predetermined offset therebetween;

10 a second latch unit for latching in parallel the  $N$  state data in response to an  $X$ -th  
11 ( $1 \leq X \leq n$ ) non-overlapped clock signal having the greatest timing margin among the first  
12 through  $n$ -th non-overlapped clock signals; and

13 a synchronizer for outputting state data from which the synchronous signal is  
detected, among data latched by the second latch unit, as restored information data, in  
response to a predetermined synchronous existence signal and the  $X$ -th non-  
overlapped clock signal,

14 wherein the first through n-th non-overlapped clock signals are generated by the  
15 phase locked loop, and each has a predetermined offset so that the clock signals are  
16 not overlapped with each other.

1 10. An optical driver in a transmitter for transmitting externally-input channel  
2 data via an optical transmission line, as an optical signal, the optical driver comprising:  
3 a bias and modulation resistance variation unit including a bias resistor and a  
4 modulation resistor, the resistance value of each of which is variable, for varying a  
5 current amount which is output due to variations in the resistance values of the bias  
6 resistor and the modulation resistor;  
a bandgap circuit for determining a bandgap reference voltage, which is always  
maintained to a constant value independently of external changes, and varying a bias  
current or a modulation current according to the determined reference voltage and  
current variations due to variations in the resistance of the bias resistor and the  
modulation resistor; and  
a laser driver for converting received channel data into current signals and  
adding the modulation current and bias current of the current signals to obtain a driving  
current for driving external optical devices.

1 11. The optical driver of claim 10, wherein the bandgap circuit comprises:  
2 a bandgap reference voltage generator for compensating according to a  
3 variation in the voltage of a first node which is a basis for voltage determination, so that  
4 the voltage of the first node is constantly maintained, and operationally amplifying  
5 between the bandgap reference voltage and a voltage at the modulation resistor and  
6 between the bandgap reference voltage and a voltage at the bias resistor to obtain first  
7 and second output voltages, respectively;  
8 a bias and modulation current generator for constantly maintaining the first and  
9 second output voltages and the voltages at the modulation resistor and the bias

10 resistor by feeding the first and second output voltages back to the bandgap reference  
11 voltage generator, and varying the modulation or bias current in response to the  
12 voltages at the modulation resistor or the bias resistor; and

13 a power save controller having at least one switch, which is switched in  
14 response to an externally-input power save control signal, the switch for converting the  
15 modes of the bandgap reference voltage generator and the bias and modulation  
16 current generator into sleep modes in response to the switching of the switches.

1 12. The optical driver of claim 10, wherein the laser driver comprises:  
2 a data separation unit for splitting the channel data into a non-inverted signal  
3 and an inverted signal to obtain a non-inverted output signal and an inverted output  
4 signal; and

5 a voltage-to-current conversion and current driving unit for calculating the  
6 voltage difference between the non-inverted output signal and the inverted output  
7 signal to obtain a current corresponding to the voltage difference, and adding the  
8 current to the bias current and the modulation current to obtain the driving current.

1 13. The optical driver of claim 10, wherein the data separation unit obtains  
2 the non-inverted output signal and the inverted output signal having the same delay  
3 time.

1 14. An optical receiver in a receiver for receiving channel data which is  
2 converted into a current signal by an external photo diode, the optical receiver  
3 comprising:

4 a bias circuit for receiving a predetermined amount of current from a power  
5 supply voltage and generating first and second bias currents;

6 a current-to-voltage converter for sourcing a current in response to the first bias  
7 current and converting a current signal received from the reception photo diode into a  
8 differential voltage signal;

9 an amplifier for sourcing a current in response to the first bias current and  
10 amplifying the differential voltage signal to obtain first and second differential output  
11 signals;

12 a duty compensator realized with different comparators having a current  
13 summing structure in which output currents are summed, the duty compensator for  
14 sourcing a current in response to the first bias current and comparing the first  
15 differential output signal with a first reference voltage and the second differential output  
16 signal with a second reference voltage to obtain first and second output signals which  
17 correspond to the compared results; and

18 a level converter for sourcing a current in response to the second bias current  
19 and digitalizing the first and second output signals by converting the voltage levels of  
20 the first and second output signals.

21 15. The optical receiver of claim 14, further comprising a buffer unit for buffering  
22 and amplifying signals received from the level converter to obtain the channel data.

23 16. The optical receiver of claim 14, wherein the optical receiver further  
24 comprises a power down controller for powering down the bias circuit so that it does not  
25 operate, in response to an externally-applied power down control signal.

26 17. The optical receiver of claim 14, wherein the duty compensator  
27 differentiates the first and second differential output signals and sets the resultant  
28 signals to be first and second reference voltages, respectively.



18. The optical receiver of claim 15, wherein the buffer unit includes a plurality of inverters which are connected to each other in series, and each of a plurality of transistors constituting the inverters is larger than the previous transistor by a multiple of  $2^K$  (where  $K$  is a natural number greater than or equal to 0).

19. A data restoration and skew compensation unit in a receiver having a phase locked loop for generating first through  $n$ -th non-overlapped clock signals, each having a predetermined offset to prevent mutual overlapping, the receiver for restoring data in which  $n$ -bit synchronous signals (where  $n$  is a positive integer greater than or equal to 1) and  $n$ -bit information data are multiplexed and transmitted in series via a transmission channel, in response to the first through  $n$ -th non-overlapped clock signals, the data restoration and skew compensation unit comprising:

a first latch unit for latching received serial data in units of  $n+N-1$  (where  $N$  is a positive integer greater than or equal to 3) bits in parallel in response to the first through  $n$ -th non-overlapped clock signals, and for outputting  $N$   $n$ -bit latched state data having the time difference of a predetermined offset therebetween;

a second latch unit for latching in parallel the  $N$  state data in response to an  $X$ -th ( $1 \leq X \leq n$ ) non-overlapped clock signal having the greatest timing margin among the first through  $n$ -th non-overlapped clock signals; and

a synchronizer for outputting state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined synchronous existence signal and the  $X$ -th non-overlapped clock signal.

20. The data restoration and skew compensation unit of claim 19, wherein the predetermined offset is the width of a unit bit constituting the serial data.

1           21.    The data restoration and skew compensation unit of claim 19, wherein the  
2 first latch unit comprises:

3               first through  $(n+N-1)$ th flip flops for data-receiving bit units constituting the  
4 received serial data, and for clock-receiving the first through  $n$ -th non-overlapped clock  
5 signals; and

6               first through  $N$ -th buffers for buffering the data output of  $n$  flip flops among the  
7 first through  $(n+N-1)$ th flip flops and outputting the buffered results as the state data.

1           22.    The data restoration and skew compensation unit of claim 19, wherein the  
2 synchronizer comprises:

3               a selector for selectively outputting the  $N$  state data in response to a selection  
4 signal;

5               a state and selection signal generator for comparing state data selected by the  
6 selector with the bit pattern of the synchronous signal in response to the sync existence  
7 signal and a current state signal representing the current state, and for outputting the  
8 selection signal and a next state signal representing the next state, in response to the  
9 results of the comparison; and

10              an  $(N+1)$ th buffer for buffering the next state signal in response to the  $X$ -th non-  
11 overlapped clock signal and outputting the result of buffering as the current state  
12 signal,

13              wherein the restored information data is state data selected by the selector when  
14 the state data is consistent with the bit pattern of the synchronous signal.

1           23.    A method of restoring information data from data in which  $n$ -bit  
2 synchronous signals (where  $n$  is a positive integer greater than or equal to 1) and the  
3  $n$ -bit information data are multiplexed and transmitted together with a clock signal in  
4 series via a transmission channel, the method comprising:

5 (a) generating first through n-th non-overlapped clock signals, each having a  
6 predetermined offset to prevent mutual overlapping, on the basis of the clock signal;

7 (b) latching received serial data in units of  $n+N-1$  (where N is a positive integer  
8 greater than or equal to 3) bits in parallel in response to the first through n-th non-  
9 overlapped clock signals;

10 A (c) generating <sup>N n-bit</sup> ~~N~~ bit-latched state data having the time difference of a  
11 predetermined offset therebetween;

12 (d) latching in parallel the N state data in synchronization with a X-th ( $1 \leq X \leq n$ )  
13 non-overlapped clock signal having the greatest timing margin among the first through  
14 n-th non-overlapped clock signals; and

15 (e) determining state data from which the synchronous signal is detected, among  
16 the latched state data, to be the restored information data, when the serial data is the  
17 synchronous signal.

18 24. The method of claim 23, wherein the step (e) comprises:

19 (e1) determining whether the first state data, which synchronizes with the clock  
20 signal, among the state data, is consistent with the bit pattern of the synchronous  
21 signal, when the serial data is the synchronous signal;

22 (e2) determining the first state data to be the restored information data, when the  
23 first state data is equal to the bit pattern;

24 (e3) determining whether the second state data, which is lagged by the  
25 predetermined offset with respect to the first state data, among the state data, is  
26 consistent with the bit pattern of the synchronous signal, if the first state data is not  
27 consistent with the bit pattern of the synchronous signal;

28 (e4) determining the second state data to be the restored information data, when  
29 the second state data is equal to the bit pattern;

30 (e5) determining whether the third state data, which leads by the predetermined  
31 offset with respect to the first state data, among the state data, is consistent with the bit

15 pattern of the synchronous signal, if the second state data is not consistent with the bit  
16 pattern of the synchronous signal;

17 (e6) determining the third state data to be the restored information data, when  
18 the third state data is equal to the bit pattern; and

19 (e7) feeding back to the step (e1) if the third state data is not consistent with the  
20 bit pattern of the synchronous signal,

21 wherein after the first, second or third state data is determined to be the restored  
22 information data, if it is not consistent with the bit pattern, the step (e1) is preformed.

007260" 8T299960